

TSMC-03-186



April 16, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/808,802 03/24/04 |

Fu-Kai Yang et al.

A TWO STEP TRENCH DEFINITION
PROCEDURE FOR FORMATION OF A DUAL
DAMASCENE OPENING IN A STACK OF
INSULATOR LAYERS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on April 26, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

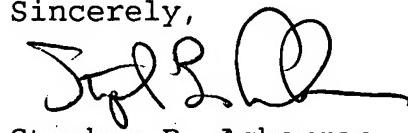
A handwritten signature in black ink, appearing to read "SBA", is written over the date "4/26/04".

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U.S. Patent 6,211,035 to Moise et al., "Integrated Circuit and Method," discusses capacitor and memory structures and fabrication methods for such structures.

U.S. Patent 6,211,063 to Liu et al., "Method to Fabricate Self-Aligned Dual Damascene Structures," describes a method to form dual damascene structures.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.